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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/385,589	08/29/1999	GARY L. GRAUNKE	42390.P7574	9393

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EXAMINER	
GURSHMAN, GRIGORY	
ART UNIT	**PAPER NUMBER**
2132	19

DATE MAILED: 03/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/385,589	GRAUNKE ET AL.	
	Examiner	Art Unit	
	Grigory Gurshman	2132	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☒ A Notice of Appeal was filed on *04 March 2004*. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *see reasons below*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *1-15 and 17-30*.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

GILBERTO BARRÓN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Applicant has not submitted any amendments.

Referring to claims 1-15 and 28-30, Applicant argues that the combination of references fails to meet prima facie case for 103(a) rejection. Applicant states that Wasilevski does not teach using the outputs of encryptor 154 as control signals to combiner 156. Examiner respectfully disagrees and points out that he uses broad but reasonable interpretation of the limitation "control signal". Wasilevskiy shows in Fig. 5 that signals from encryptor is being input in combiner where it controls the process.

Examiner maintains that the combination of Wasilevskiy and Richard meets the prima facie case of obviousness because, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the combiner coupled to a data bit generator of Wasilewski by adding the shuffle units as taught in Richard. One of ordinary skill in the art would have been motivated to modify the combiner coupled to a data bit generator by adding the shuffle units as taught in Richard for providing the fully encoded signal (see Richard, abstract and column 2, lines 56-60).

Referring to claims 17-27, Applicant argues that the combination of references fails to meet prima facie case for 103(a) rejection. Examiner mainains his position and points out that Shukla teaches XOR operations along with shuffling data blocks (see column 2, lines 55-56). Referring to the independent claim 17, the limitation "a first XOR gate to receive a first plurality of data bits and combine them into a second data bit" is met by XOR operation of the data block D with the string S to obtain a new data block D1(see column 3, lines 12-14). The limitation "a network of shuffle units, coupled to the first XOR gate, to output a third data bit by shuffling and propagating the second data bit through the network of shuffle units" is met by the second operation, which shuffles the bits of the data block D1 to obtain a new data block D2 (see column 3, lines 14 -16). The limitation " a second XOR gate coupled to the network of shuffle units to combine a fifth plurality of data bits using the third data bit" is met by the a second type of XOR that uses the bits of the data block D2 and produces the data block D3 (see column 3, lines 16-18). Shukla explicitly shows the limitations, recited in the independent claim 17, in Fig. 3. Shukla shows the use of shuffle units (see Fig. 3). Shukla, however, does not explicitly teach shuffle unit comprising flip-flops for state values. Richard teaches the means for combining the generated bit sequence with a clear text data bit signal and shuffling means, which receives the encoded signal and shuffles the positions of the bits within the signal (see column 2, lines 50 -57 and Fig. 4A unit 160). Richard also teaches a shuffle unit, which comprises flip-flops (see unit 164 in Fig 4A and units 73 and 74 in Fig 2A) coupled to selectors (units 70, 71, 75 and 72 in Fig 2A). Therefore, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the shuffle units coupled to XOR gates of Shukla by adding the flip-flops coupled to the selectors as taught in Richard. One of ordinary skill in the art would have been motivated to modify the shuffle units coupled to XOR gates by adding the flip-flops coupled to the selectors as taught in Richard for controlling the mode of operation of Shuffle Register.

Claims 1-15 and 17-30 stand rejected per Final Office action.